What is claimed is:

1. A non-volatile memory system comprising:

at least one non-volatile memory device, wherein the at least one non-volatile memory device contains a memory array with a plurality of physical row pages arranged in a plurality of erase blocks, wherein each physical row page containing one or more user data sectors and one or more overhead data areas; and

wherein a non-split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block to a target erase block in a modified copy-back move operation such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of the target erase block by reading the selected user data sectors and the associated overhead data areas into an internal latch of the at least one non-volatile memory device, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page.

2. The non-volatile memory system of claim 1, wherein an interface to the non-volatile memory system is compatible with a mass storage device.

3. The non-volatile memory system of claim 1, wherein an interface to the non-volatile memory system is one of a PCMCIA-ATA, a Compact Flash (CF), a USB Flash, and a multimedia card (MMC) compatible interface.

4. The non-volatile memory system of claim 1, wherein one or more non-volatile memory devices of the non-volatile memory system are one of a NOR architecture Flash memory device, a NAND architecture Flash memory device, a Polymer memory device, a Ferroelectric Random Access Memory (FeRAM) memory device, a Ovionics Unified Memory (OUM) memory device, and a Magnetoresistive Random Access Memory (MRAM) memory device.

5. The non-volatile memory system of claim 1, wherein each user data sector contains 512 bytes.

6. The non-volatile memory system of claim 1, wherein each associated overhead data area contains an error correction code (ECC).

7. The non-volatile memory system of claim 6, wherein the non-split data move control circuit is adapted to evaluate the associated ECC codes as data is moved.

8. A non-volatile memory system comprising:

at least one non-volatile memory device, wherein the at least one non-volatile memory device contains a memory array with a plurality of physical row pages arranged in a plurality of erase blocks, wherein the erase blocks of the at least one non-volatile memory device are arranged in pairs into a plurality of super blocks and each physical row page containing one or more user data sectors and one or more overhead data areas; and

wherein a split data move control circuit is adapted to move one or more selected user data sectors stored in two or more physical row pages of a selected source super block to a target super block such that the selected user data sectors stored in a first source physical row page of the source super block are moved to a first target physical row page of the target super block and the associated overhead data areas of the selected user data sectors stored in a second source physical row page of the source super block are

moved to a second target physical row page of the target super block.

9. The non-volatile memory system of claim 8, wherein the split data move control circuit is adapted to move data between the source and target super blocks, where the source and target super blocks are in the same non-volatile memory device.

10. The non-volatile memory system of claim 8, wherein the split data move control circuit is adapted to move data between the source and target super blocks, where the source and target super blocks are in differing non-volatile memory devices.

11. The non-volatile memory system of claim 8, wherein an interface to the non-volatile memory system is compatible with a mass storage device.

12. The non-volatile memory system of claim 8, wherein an interface to the non-volatile memory system is one of a PCMCIA-ATA, a Compact Flash (CF), a USB Flash, and a multimedia card (MMC) compatible interface.

13. The non-volatile memory system of claim 8, wherein one or more non-volatile memory devices of the non-volatile memory system are one of a NOR architecture Flash memory device, a NAND architecture Flash memory device, a Polymer memory device, a Ferroelectric Random Access Memory (FeRAM) memory device, a Ovionics Unified Memory (OUM) memory device, and a Magnetoresistive Random Access Memory (MRAM) memory device.

14. The non-volatile memory system of claim 8, wherein each associated overhead data area contains an error correction code (ECC).

15. The non-volatile memory system of claim 14, wherein the split data move control circuit is adapted to evaluate the associated ECC codes as data is moved.

16. A Flash memory system comprising:

at least one Flash memory device, wherein the at least one Flash memory device contains a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of physical row pages, each physical row page containing one or more user data sectors and one or more overhead data areas;

wherein the erase blocks of the at least one Flash memory device are arranged in pairs into a plurality of super blocks;

a control circuit adapted to control data accesses to the sectors of the erase block pair of a selected super block such that user data access and overhead data accesses are directed to differing erase blocks of the super block; and

wherein a split data move control circuit is adapted to move one or more selected user data sectors stored in two or more physical row pages of an erase block pair of a selected source super block such that the selected user data sectors stored in a first source physical row page of a first erase block of the source super block are moved to a first target physical row page of a first erase block of a target super block and the associated overhead data areas of the selected user data sectors stored in a second source physical row page of a second erase block of the source super block are moved to a second target physical row page of a second erase block of the target super block.

17. The Flash memory system of claim 16, wherein the split data move control circuit is adapted to move data between the source and target super blocks, where the source and target super blocks are in the same non-volatile memory device.

18. The Flash memory system of claim 16, wherein the split data move control circuit is adapted to move data between the source and target super blocks,

where the source and target super blocks are in differing non-volatile memory devices.

19. The Flash memory system of claim 16, wherein the split data move control circuit is adapted to evaluate an error correction code (ECC) stored in each associated overhead data area as data is moved.

20. The Flash memory system of claim 16, wherein the split data move control circuit is adapted to read data with a NAND Flash read command.

21. The Flash memory system of claim 16, wherein the split data move control circuit is adapted to read data with a NAND Flash modified data write command.

22. The Flash memory system of claim 16, wherein the split data move control circuit is adapted to mask a selected range of data column bit values in an internal data latch by masking a pre-count range of undesired column bit values and masking a post-count range of undesired data column bit values.

23. The Flash memory system of claim 22, wherein the split data move control circuit is adapted to mask by masking the pre-count range starting from a column address zero in the source physical page and masking a post-count range starting from a selected post column address in the source physical page.

24. The Flash memory system of claim 22, wherein the split data move control circuit is adapted to mask a selected range of data column bit values in the internal data latch by inserting logical 1's into the internal data latch to replace unwanted data.

25. A non-volatile memory device comprising:
a memory array containing a plurality of memory cells arranged into a plurality

of sectors in a plurality of erase blocks, wherein the erase blocks are arranged in pairs into a plurality of super blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of physical row pages, each physical row page containing one or more user data sectors and one or more overhead data areas;

a control circuit, wherein the control circuit is adapted to perform data accesses to the sectors of the erase block pair of a super block such that user data access and overhead data accesses are directed to differing erase blocks of the super block; and

a split data move control circuit, wherein the split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in two or more physical row pages of an erase block pair of a selected source super block such that the selected user data sectors stored in a first source physical row page of a first erase block of the source super block are moved to a first target physical row page of a first erase block of a target super block and the associated overhead data areas of the selected user data sectors stored in a second source physical row page of a second erase block of the source super block are moved to a second target physical row page of a second erase block of the target super block.

26. The non-volatile memory device of claim 25, wherein the non-volatile memory device is one of a NOR architecture Flash memory device, a NAND architecture Flash memory device, a Polymer memory device, a Ferroelectric Random Access Memory (FeRAM) memory device, a Ovionics Unified Memory (OUM) memory device, and a Magnetoresistive Random Access Memory (MRAM) memory device.

27. The non-volatile memory device of claim 25, wherein the split data move control circuit is adapted to evaluate an error correction code (ECC) stored in each associated overhead data area as data is moved.

28. The non-volatile memory device of claim 27, further comprising:

a pair of internal data latches, wherein the split data move control circuit is adapted to store the one or more selected user data sectors of the first source physical row in a first internal data latch and the one or more associated overhead data areas of the second source physical row to allow for the error correction code (ECC) for each user data sector and associated overhead data area to be evaluated and the data corrected as necessary before written to the target super block.

29. A non-volatile memory controller comprising:

a control circuit coupled to a host interface;

a memory device interface for one or more non-volatile memory devices coupled to the memory control circuit, wherein each of the one or more non-volatile memory devices has a memory array containing a plurality of memory cells arranged into a plurality of sectors in a plurality of erase blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of physical row pages, each physical row page containing one or more user data sectors and one or more overhead data areas;

wherein the control circuit is adapted to perform data accesses to the sectors of the plurality of erase blocks of the one or more non-volatile memory devices; and

a non-split data move control circuit, wherein the non-split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block of the one or more non-volatile memory devices such that the selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of a target erase block by reading the

selected user data sectors and the associated overhead data areas into an internal latch of the one or more non-volatile memory devices, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page.

30. The non-volatile memory controller of claim 29, wherein the non-volatile memory controller is adapted to control one of a NOR architecture Flash memory device, a NAND architecture Flash memory device, a Polymer memory device, a Ferroelectric Random Access Memory (FeRAM) memory device, a Ovionics Unified Memory (OUM) memory device, and a Magnetoresistive Random Access Memory (MRAM) memory device.

31. The non-volatile memory controller of claim 29, wherein the non-volatile memory controller is adapted to present an interface that is compatible with a mass storage device.

32. The non-volatile memory controller of claim 29, wherein each associated overhead data area contains an error correction code (ECC).

33. The non-volatile memory controller of claim 32, wherein the non-split data move control circuit is adapted to evaluate the one or more selected user data sectors and their associated ECC codes as data is moved.

34. The non-volatile memory controller of claim 33, wherein the non-split data move control circuit is adapted to respond to detecting an unfixable error by one of alerting a data failure in the memory system, marking an affected sector as corrupt, and doing nothing.

35. The non-volatile memory controller of claim 33, wherein the split data move control circuit is adapted to respond to detecting a fixable error by one of fixing the error in the internal latch before writing to the target physical row page, fixing the error and writing to a new target physical row page, and doing nothing.

36. A non-volatile memory controller comprising:

a control circuit coupled to a host interface;

a memory device interface for one or more non-volatile memory devices coupled to the memory control circuit, wherein each of the one or more non-volatile memory devices has a memory array containing a plurality of memory cells arranged into a plurality of sectors in a plurality of erase blocks, wherein the erase blocks are arranged in pairs into a plurality of super blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of physical row pages, each physical row page containing one or more user data sectors and one or more overhead data areas;

wherein the control circuit is adapted to perform data accesses to the sectors of the erase block pair of a super block of the one or more non-volatile memory devices such that user data access and overhead data accesses are directed to differing erase blocks of the super block; and

a split data move control circuit, wherein the split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in two or more physical row pages of an erase block pair of a selected source super block of the one or more non-volatile memory devices such that the selected user data sectors stored in a first source physical row page of a first erase block of the source super block are moved to a first target physical row page of a first erase block of a target super block and the associated overhead data areas of the selected user data

sectors stored in a second source physical row page of a second erase block of the source super block are moved to a second target physical row page of a second erase block of the target super block.

37. The non-volatile memory controller of claim 36, wherein the control circuit is adapted to sequentially access physical sectors of the first and second erase blocks in a pattern that alternates between physical row pages of a first and a second erase block of each super block as the physical sectors of the super block are sequentially accessed.

38. The non-volatile memory controller of claim 36, wherein the non-volatile memory controller is adapted to control one of a NOR architecture Flash memory device, a NAND architecture Flash memory device, a Polymer memory device, a Ferroelectric Random Access Memory (FeRAM) memory device, a Ovionics Unified Memory (OUM) memory device, and a Magnetoresistive Random Access Memory (MRAM) memory device.

39. The non-volatile memory controller of claim 36, wherein the non-volatile memory controller is adapted to present an interface that is compatible with a mass storage device.

40. The non-volatile memory controller of claim 36, wherein each associated overhead data area contains an error correction code (ECC).

41. The non-volatile memory controller of claim 40, wherein the split data move control circuit is adapted to evaluate the one or more selected user data sectors and their associated ECC codes as data is moved.

42. The non-volatile memory controller of claim 41, wherein the split data move control circuit is adapted to respond to detecting an unfixable error by one of

alerting a data failure in the memory system, marking an affected sector as corrupt, and doing nothing.

43. The non-volatile memory controller of claim 41, wherein the split data move control circuit is adapted to respond to detecting a fixable error by one of fixing the error and writing to a new target physical row page, and doing nothing.

44. A non-split data move control circuit comprising:
a control circuit, wherein the control circuit is adapted to receive a non-split user and overhead data move request, command one or more user data sectors and associated overhead data areas of a source physical row page of a source erase block to be read into an internal latch of a non-volatile memory device, command transferring one or more latched user data sectors and associated overhead data areas from the non-volatile memory device, command the masking of the one or more user data sectors and associated overhead data areas in the internal latch, and command writing the one or more user data sectors and associated overhead data areas to a target physical row page of a target erase block.

45. A split data move control circuit comprising:
a control circuit, wherein the control circuit is adapted to receive a split user and overhead data move request and read one or more user data sectors of a source physical row page of a first erase block of a source erase block pair and write the one or more user data sectors to a target physical row page of a first erase block of a target erase block pair, and read one or more associated overhead data codes from a source physical row page of a second erase block of the source erase block pair and write the one or more associated overhead data codes to a target physical row page of a second erase block of the target erase block pair.

46. A NAND architecture Flash memory non-split data move control circuit comprising:

a control circuit coupled to a NAND command circuit, a target row register, a source Pre-Count Counter, a source Post Address Register, and a source Post-Count Counter;

wherein a microprocessor interface, an automation control interface, an external address generation hardware interface, and a NAND Flash interface are coupled to the non-split data move control circuit; and

wherein the non-split data move control circuit is adapted to read one or more user data sectors and/or ECC codes of a source physical row page of a source erase block of a NAND architecture Flash memory device and write the one or more user data sectors and/or ECC codes to a target physical row page of a target erase block addressed by the target row register, where the non-split data move control circuit is adapted to transfer the one or more user data sectors and/or ECC codes from the NAND architecture Flash memory device, and where the non-split data move control circuit is adapted to mask a selected range of read data as it is held in a data latch.

47. The NAND architecture Flash memory non-split data move control circuit of claim 46, wherein the non-split data move control circuit is adapted to read data with a NAND Flash read command.

48. The NAND architecture Flash memory non-split data move control circuit of claim 46, wherein the non-split data move control circuit is adapted to write data with a NAND Flash modified data write command.

49. The NAND architecture Flash memory non-split data move control circuit of claim 46, wherein the non-split data move control circuit is adapted to mask out a pre-count range of undesired column bit values stored in the Pre-Count Counter and a post-count range of undesired data column bit values stored in the

Post-Count Counter.

50. The NAND architecture Flash memory non-split data move control circuit of claim 49, wherein the split data move control circuit is adapted to mask out the pre-count range starting from column address zero in the source physical page and is adapted to mask out the post-count range starting from a selected post column address stored in the Post Address Register.

51. The NAND architecture Flash memory non-split data move control circuit of claim 46, wherein the selected range of data column bit values in the data latch are masked out the selected range of data by inserting data comprising logical 1's into the data latch to replace unwanted data.

52. The NAND architecture Flash memory non-split data move control circuit of claim 46, wherein the non-split data move control circuit is adapted to utilize a NAND Flash status command to check for NAND Flash memory device command completion.

53. The NAND architecture Flash memory non-split data move control circuit of claim 46, wherein the non-split data move control circuit is adapted to utilize a Ready/Busy (R/B#) signal line to check for NAND Flash memory device command completion.

54. A NAND architecture Flash memory split data move control circuit comprising:

a control circuit coupled to a NAND command circuit, an A and B target row registers, a source A and B Pre-Count Counters, a source A and B Post Address Register, and a source A and B Post-Count Counters;

wherein a microprocessor interface, an automation control interface, an external address generation hardware interface, and a NAND Flash interface are coupled to the split data move control circuit; and

wherein the split data move control circuit is adapted to read one or more user data sectors and/or ECC codes of a source A physical row page of a first erase block of a source erase block pair and write the one or more user data sectors and/or ECC codes to a target A physical row page of a first erase block of a target erase block pair addressed by the target A row register, and read one or more user data sectors and/or ECC codes from a source B physical row page of a second erase block of the source erase block pair and write the one or more user data sectors and/or ECC codes to a target B physical row page of a second erase block of the target erase block pair addressed by the target B row register.

55. The NAND architecture Flash memory split data move control circuit of claim 54, wherein the split data move control circuit is adapted to read data with a NAND Flash read command.

56. The NAND architecture Flash memory split data move control circuit of claim 54, wherein the split data move control circuit is adapted to write data with a NAND Flash modified data write command.

57. The NAND architecture Flash memory split data move control circuit of claim 54, wherein the split data move control circuit is adapted to mask a selected range of read data as it is held in a data latch.

58. The NAND architecture Flash memory split data move control circuit of claim 57, wherein the split data move control circuit is adapted to mask out a pre-count range of undesired column bit values stored in the A or B Pre-Count Counter and a post-count range of undesired data column bit values stored in the A or B Post-Count Counter.

59. The NAND architecture Flash memory split data move control circuit of claim

58, wherein the split data move control circuit is adapted to mask out the pre-count range starting from column address zero in the source physical page and is adapted to mask out the post-count range starting from a selected post column address stored in the A or B Post Address Register.

60. The NAND architecture Flash memory split data move control circuit of claim 57, wherein the selected range of data column bit values in the data latch are masked out the selected range of data by inserting data comprising logical 1's into the data latch to replace unwanted data.

61. The NAND architecture Flash memory split data move control circuit of claim 54, wherein the split data move control circuit is adapted to utilize a NAND Flash status command to check for NAND Flash memory device command completion.

62. The NAND architecture Flash memory split data move control circuit of claim 54, wherein the split data move control circuit is adapted to utilize a Ready/Busy (R/B#) signal line to check for NAND Flash memory device command completion.

63. A method of operating a non-volatile memory system comprising:

reading data of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices;

transferring selected data from the selected non-volatile memory device;

masking off a first selected range of data column bit values; and

writing the first selected range of data column bit values to a physical page row of a target erase block.

64. The method of claim 63, wherein reading data of a physical page row of a source erase block from a selected non-volatile memory device of one or more

non-volatile memory devices further comprises reading data of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices where the selected non-volatile memory device comprises one of a NOR architecture Flash memory device, a NAND architecture Flash memory device, a Polymer memory device, a Ferroelectric Random Access Memory (FeRAM) memory device, a Ovionics Unified Memory (OUM) memory device, and a Magnetoresistive Random Access Memory (MRAM) memory device.

65. The method of claim 63, wherein masking off a selected range of data column bit values further comprises masking off a pre-count range of undesired column bit values and a post-count range of undesired data column bit values.

66. The method of claim 65, wherein masking off a pre-count range and a post-count range further comprises masking off a pre-count range starting from column address zero in the source physical page and masking off a post-count range starting from a selected post column address in the source physical page.

67. The method of claim 63, wherein masking a selected range of data column bit values further comprises masking out a selected range of data by inserting logical 1's.

68. The method of claim 63, further comprising:
presenting an interface to the non-volatile memory system compatible with a mass storage device.

69. A method of operating a split data non-volatile memory system comprising:
reading data of a physical page row of a first source erase block of a source super block from a selected non-volatile memory device of one or more non-volatile memory devices;

masking off a first selected range of data column bit values;

writing the first selected range of data column bit values to a physical page row of a first target erase block of a target super block;

reading data of a physical page row of a second source erase block of the source super block;

masking off a second selected range of data column bit values; and

writing the second selected range of data column bit values to a physical page row of a second target erase block of the target super block.

70. The method of claim 69, wherein reading data of a physical page row of a first source erase block of a source super block from a selected non-volatile memory device of one or more non-volatile memory devices further comprises reading data of a physical page row of a first source erase block of a source super block from a selected non-volatile memory device of one or more non-volatile memory devices where the selected non-volatile memory device comprises one of a NOR architecture Flash memory device, a NAND architecture Flash memory device, a Polymer memory device, a Ferroelectric Random Access Memory (FeRAM) memory device, a Ovionics Unified Memory (OUM) memory device, and a Magnetoresistive Random Access Memory (MRAM) memory device.

71. The method of claim 69, wherein masking off a selected range of data column bit values further comprises masking off a pre-count range of undesired column bit values and a post-count range of undesired data column bit values.

72. The method of claim 71, wherein masking off a pre-count range and a post-count range further comprises masking off a pre-count range starting from column address zero in the source physical page and masking off a post-count range starting from a selected post column address in the source physical page.

73. The method of claim 69, wherein masking a selected range of data column bit values further comprises masking out a selected range of data by inserting logical 1's.

74. The method of claim 69, further comprising:
presenting an interface to the data splitting non-volatile memory system compatible with a mass storage device.

75. A method of operating a split data non-volatile memory system comprising:
reading one or more user data sectors of a physical page row of a first source erase block of a source super block from a selected non-volatile memory device of one or more non-volatile memory devices;
writing the one or more user data sectors to a physical page row of a first target erase block of a target super block;
reading one or more overhead data areas of a physical page row of a second source erase block of the source super block; and
writing the one or more overhead data areas to a physical page row of a second target erase block of a target super block.

76. The method of claim 75, wherein writing the one or more user data sectors their associated overhead data areas to the target super block further comprises writing the one or more user data sectors and their associated overhead data areas to the target super block, where the source and target super blocks are in the same non-volatile memory device.

77. The method of claim 75, wherein writing the one or more user data sectors their associated overhead data areas to the target super block further comprises writing the one or more user data sectors and their associated overhead data areas to the target super block, where the source and target super blocks are in differing non-volatile memory devices.

78. The method of claim 75, wherein reading one or more overhead data areas of a physical page row of a second source erase block of the source super block further comprises reading one or more overhead data areas of a physical page row of a second source erase block of the source super block, where each associated overhead data area contains an error correction code (ECC).

79. The method of claim 78, further comprising:
evaluating the one or more user data sectors their associated ECC codes for data errors as data is moved.

80. The method of claim 79, wherein evaluating the one or more user data sectors and their associated ECC codes for data errors as data is moved further comprises evaluating the one or more user data sectors and their associated ECC codes for data errors as data is moved, where the response to detecting an unfixable error is one of alerting a data failure in the memory system, marking an affected sector as corrupt, and doing nothing.

81. The method of claim 79, wherein evaluating the one or more user data sectors and their associated ECC codes for data errors as data is moved further comprises evaluating the one or more user data sectors and their associated ECC codes for data errors as data is moved, where the response to detecting a fixable error is one of fixing the error and writing to a new target physical row page, and doing nothing.

82. The method of claim 79, further comprising:
storing the one or more user data sectors before writing them to a physical page row of a first target erase block of a target super block until their associated ECC codes can be read and evaluated against the stored one or more user data sectors and any possible data corrections made.

83. A method of moving data in a memory system comprising:

reading one or more user data sectors and one or more overhead data areas of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices;

transferring selected data of the one or more user data sectors and one or more overhead data areas from the selected non-volatile memory device;

masking the one or more user data sectors and one or more overhead data areas; and

writing the one or more user data sectors and one or more overhead data areas to a physical page row of a target erase block.

84. A method of moving split data in a memory system comprising:

reading one or more user data sectors of a physical page row of a first source erase block of a source super block from a selected non-volatile memory device of one or more non-volatile memory devices;

writing the one or more user data sectors to a physical page row of a first target erase block of a target super block;

reading one or more overhead data areas of a physical page row of a second source erase block of the source super block; and

writing the one or more overhead data areas to a physical page row of a second target erase block of a target super block.

85. A system comprising:

a host coupled to a Flash memory system, wherein the Flash memory system comprises:

at least one Flash memory device, wherein the at least one Flash memory device contains a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of physical row

pages, each physical row page containing one or more user data sectors and one or more overhead data areas;

a control circuit adapted to control data accesses to the sectors of a selected erase block; and

wherein a non-split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of the selected source erase block to a target erase block in a modified copy-back move operation such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of the target erase block by reading the selected user data sectors and the associated overhead data areas into an internal latch of the at least one Flash memory device, transferring one or more latched user data sectors and associated overhead data areas from the at least one Flash memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page.

86. The system of claim 85, wherein the Flash memory system is adapted to appear to the host as a rewriteable storage device.

87. The system of claim 85, wherein the host is one of a processor and an external memory controller.

88. The system of claim 85, wherein an interface to the Flash memory system is compatible with a mass storage device.

89. A system comprising:

a host coupled to a Flash memory system, wherein the Flash memory system

comprises:

at least one Flash memory device, wherein the at least one Flash memory device contains a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, and wherein each erase block of the plurality of erase blocks contains a plurality of physical row pages, each physical row page containing one or more user data sectors and one or more overhead data areas;

wherein the erase blocks of the at least one Flash memory device are arranged in pairs into a plurality of super blocks;

a control circuit adapted to control data accesses to the sectors of the erase block pair of a selected super block such that user data access and overhead data accesses are directed to differing erase blocks of the super block; and

wherein a split data move control circuit is adapted to move one or more selected user data sectors stored in two or more physical row pages of an erase block pair of a selected source super block such that the selected user data sectors stored in a first source physical row page of a first erase block of the source super block are moved to a first target physical row page of a first erase block of a target super block and the associated overhead data areas of the selected user data sectors stored in a second source physical row page of a second erase block of the source super block are moved to a second target physical row page of a second erase block of the target super block.

90. The system of claim 89, wherein the Flash memory system is adapted to appear to the host as a rewriteable storage device.

91. The system of claim 89, wherein the host is one of a processor and an external memory controller.

92. The system of claim 89, wherein an interface to the Flash memory system is compatible with a mass storage device.

93. A method of moving data in a split data NAND architecture Flash memory system comprising:

reading data of a physical page row of a first source erase block of a source super block from a selected NAND architecture Flash device of one or more non-volatile memory devices into an internal data latch;

writing the data by:

masking off a first selected range of data column bit values in the internal data latch, and

writing the first selected range of data column bit values in the internal data latch to a physical page row of a first target erase block of a target super block of the selected NAND architecture Flash memory device;

reading data of a physical page row of a second source erase block of the source super block into the internal data latch; and

writing the data by:

masking off a second selected range of data column bit values in the internal data latch, and

writing the second selected range of data column bit values from the internal data latch to a physical page row of a second target erase block of the target super block.

94. The method of claim 93, wherein reading data further comprises reading data with a NAND Flash read command.

95. The method of claim 93, wherein writing data further comprises writing data with a NAND Flash modified data write command.

96. The method of claim 93, wherein masking a selected range of data column bit

values in the internal data latch further comprises masking out a pre-count range of undesired column bit values and a post-count range of undesired data column bit values.

97. The method of claim 96, wherein masking out a pre-count range and a post-count range further comprises masking out a pre-count range starting from column address zero in the source physical page and masking out a post-count range starting from a selected post column address in the source physical page.

98. The method of claim 93, wherein masking a selected range of data column bit values in the internal data latch further comprises masking out a selected range of data by inserting 1's into the internal data latch to replace unwanted data.

99. The method of claim 93, wherein reading and writing the data further comprise reading and writing the data utilizing a NAND Flash status command to check for read and/or write command completion.

100. The method of claim 93, wherein reading and writing the data further comprise reading and writing the data utilizing a Ready/Busy (R/B#) signal line to check for read and/or write command completion.

101. A non-volatile memory system comprising:

at least one non-volatile memory device, wherein the at least one non-volatile memory device contains a memory array with a plurality of physical row pages arranged in a plurality of erase blocks, wherein each physical row page contains one or more user data sectors and one or more overhead data areas; and

wherein a data move control circuit has a means for moving one or more selected user data sectors and one or more associated overhead areas stored in one or more physical row pages of a selected source erase block to a

target erase block such that the selected user data sectors and associated overhead areas are masked and transferred from the at least one non-volatile memory device as they are moved.

102. A non-volatile memory system comprising:

at least one non-volatile memory device, wherein the at least one non-volatile memory device contains a memory array with a plurality of physical row pages arranged in a plurality of erase blocks, wherein the erase blocks of the at least one non-volatile memory device are arranged in pairs into a plurality of super blocks and each physical row page containing one or more user data sectors and one or more overhead data areas; and

wherein a split data move control circuit has a means for moving one or more selected user data sectors stored in two or more physical row pages of a selected source super block to a target super block such that the selected user data sectors stored in a first source physical row page of the source super block are moved to a first target physical row page of the target super block and the associated overhead data areas of the selected user data sectors stored in a second source physical row page of the source super block are moved to a second target physical row page of the target super block.